

DM54259/DM74259 8-Bit Addressable Latches

General Description

These 8-bit addressable latches are designed for general purpose storage applications in digital systems. Specific uses include working registers, serial-holding registers, and active-high decoders or demultiplexers. They are multifunctional devices capable of storing single-line data in eight addressable latches, and being a 1-of-8 decoder or demultiplexer with active-high outputs.

Four distinct modes of operation are selectable by controlling the clear and enable inputs as enumerated in the function table. In the addressable-latch mode, data at the datain terminal is written into the addressed latch. The addressed latch will follow the data input with all unaddressed latches remaining in their previous states. In the memory mode, all latches remain in their previous states and are unaffected by the data or address inputs. To eliminate the possibility of entering erroneous data in the latches, the enable should be held high (inactive) while the address lines are changing. In the 1-of-8 decoding or demultiplexing mode, the addressed output will follow the level of the D input with all other outputs low. In the clear mode, all outputs are low and unaffected by the address and data inputs.

Features

- 8-bit parallel-out storage register performs serial-to-parallel conversion with storage
- Asynchronous parallel clear
- Active high decoder
- Enable/disable input simplifies expansion
- Direct replacement for Fairchild 9334
- Expandable for N-bit applications
- Four distinct functional modes
- Typical propagation delay times: Enable-to-output 18 ns Data-to-output 21 ns Address-to-output 22 ns Clear-to-output 21 ns
- Fan-Out

 I_{OL} (sink current) 16 mA

 I_{OH} (source current) −0.8 mA
- Typical I_{CC} 60 mA

Connection Diagram

V_{CC} CLEAR Ē D Q7 Q6 Q5 Q4

Dual-In-Line Package

Order Number DM54259J or DM74259N See NS Package Number J16A or N16A

Q1

02

03

GND

an

TL/F/6569-1

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage 7V Input Voltage 5.5V

Operating Free Air Temperature Range

DM54 -55°C to +125°C DM74 0°C to +70°C

Storage Temperature Range $-65^{\circ}\text{C to} + 150^{\circ}\text{C}$

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Cumbal	Parameter Supply Voltage		DM54259			DM74259			Units
Symbol			Min N	Nom	Max	Min	Nom	Max	Jints
Vcc			4.5	5	5.5	4.75	5	5.25	٧
V _{IH}	High Level Input Voltage		2			2			V
V _{IL}	Low Level Input Voltage				0.8			8.0	٧
ЮН	High Level Output Current				-0.8			-0.8	mA
loL	Low Level Output Current				16			16	mA
tw	Pulse Width (Note 6)	Enable	19	13		19	13		ns
		Clear	19	13		19	13		
tsu	Setup Time	Data	20	13		20	13		ns
	(Notes 1, 2, 3 & 6)	Select	10	5		10	5		
111	Hold Time (Notes 1 & 6)	Data	0	-10		0	-10		ns
		Select	0	-13		0	-13		115
TA	Free Air Operating Temperature		-55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 3)	Max	Units
VI	Input Clamp Voltage	$V_{CC} = Min, I_{\dagger} = -12 \text{ mA}$				-1.5	٧
V _{OH}	High Level Output Voltage	$V_{CC} = Min, I_{OH} = Max$ $V_{IL} = Max, V_{IH} = Min$		2.4	3.4		٧
V _{OL}	Low Level Output Voltage	$V_{CC} = Min, I_{OL} = Max$ $V_{IH} = Min, V_{IL} = Max$			0.2	0.4	V
l _l	Input Current @ Max Input Voltage	$V_{CC} = Max, V_I = 5.5V$				1	mA
l _{IH}	High Level Input Current	$V_{CC} = Max, V_I = 2.4V$				40	μΑ
ήլ <u>L</u>	Low Level Input Current	$V_{CC} = Max, V_I = 0.4V$				-1.6	mA
los	Short Circuit	V _{CC} = Max DM54		-20		-55	mA
	Output Current	(Note 4)	DM74 -20			-55	
lcc	Supply Current	V _{CC} = Max (Note 5)				90	mA

Note 1: Setup and hold times are with reference to the enable input.

Note 2: The select-to-enable setup time is the time before the High-to-Low enable transition that the select must be stable so that the correct latch is selected and the others not affected.

Note 3: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 4: Not more than one output should be shorted at a time.

Note 5: I_{CC} is measured with 4.5V applied to all inputs and all outputs open.

Note 6: $T_A = 25^{\circ}C$ and $V_{CC} = 5V$.

Switching	Characteristics at V _{CC} = 5V and T _A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input)	$R_L = 400\Omega$	Units	
		To (Output)	Min	Max	Units
^t PLH	Propagation Delay Time Low to High Level Output	Enable to Output		28	ns
[†] PHL	Propagation Delay Time High to Low Level Output	Enable to Output		27	ns
t _{PLH}	Propagation Delay Time Low to High Level Output	Data to Output		35	ns
^t PHL	Propagation Delay Time High to Low Level Output	Data to Output		28	ns
^t PLH	Propagation Delay Time Low to High Level Output	Select to Output		35	ns
t _{PHL}	Propagation Delay Time High to Low Level Output	Select to Output		35	ns
t _{PHL}	Propagation Delay Time High to Low Level Output	Clear to Output		31	ns

Function Tables

Inputs		Output of Addressed	Each Other	Function
Clear	Ē	Latch	Output	
Н	L	D	Q _{i0}	Addressable Latch
н	Н	Q _{i0}	Q _{iO}	Memory
L	L	D	L	8-Line Demultiplexer
L	н	L	L	Clear

Latch Selection Table

Se	lect Inpu	Latch		
С	В	A	Addressed	
L	L	L	0	
L	L	H	1	
L	Н	L	2	
L	Н	н	3	
Н	L	L	4	
Н	L	н	5	
Н	Н	L	6	
Н	Н	Н	7	

H = High Level, L = Low Level

D = The level of the data input

 $Q_{i0}=$ The level of Q_i (i $=0,\,1,\,\ldots\,7,$ as appropriate) before the indicated steady-state input conditions were established.